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EXAMINER	
TRUJILLO, JAMES K	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 07/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/863,103	LAMBINO ET AL.	
	Examiner	Art Unit	
	James K. Trujillo	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated 4/11/05.

2. Claims 1-25 are presented for examination.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. The rejections with respect to claims 17-25 are respectfully maintained and reproduced infra for applicant's convenience.

5. Regarding claim 20, Miller teaches a system comprising:

a. a processor (CPU) [col. 4 lines 45-49];

b. a flash memory comprising a primary location (first writable segment/first region) and a secondary location (second writable segment/second region, col. 3 lines 31-36, col. 5 line 45 through col. 6 line 10 and figure 3); and

c. a boot block executed from the primary location wherein the boot block further:

i. is copied to the secondary location (col. 3 lines 31-36, col. 5 line 45 through col. 6 line 10 and figure 3);

ii. modifies an address bit (a flag such as hardware sticky bit) of an execution address to point to the secondary location (col. 5 line 65 through col. 6 line 2 and col. 7, lines 4-42).

iii. maintains the state of the modified address bit of the execution address following a power cycle (if a reset occurs the flag will still be set, col. 6 lines 4-9); and

iv. copies a new boot block (update first block) to the primary location [figure 3 and col. 5 line 65 et seq.]

v. points the execution address to the primary location (the PC will be allowed to boot from code in the primary location, therefore the execution address must point to the primary location, col. 7 lines 4-7).

6. Regarding claim 21, Miller teaches the system according to claim 20, as described above. Miller further teaches an address conversion mechanism (boot in progress flag) for moving the execution address (flag determines where execution will begin, col. 6 lines 2-10 and col. 7 lines 4-7).

7. Regarding claims 17 and 24, Miller taught the claimed system according to claim 20. Therefore, Miller also teaches the claimed method of using and the claimed article comprising a medium for storing instructions to enable such a system as the limitations of the method and the article appear to be same as that of the system.

8. Regarding claim 18, Miller taught the method according to claim 17 as described above. Miller further taught wherein pointing an execution address to the secondary location further comprising inverting an address bit of the execution address (col. 6 lines 2-10 and col. 7 lines 4-42). Specifically, Miller discloses using a bit to determine where the execution address is pointed. If the bit is set (a "1") the execution address will point to the secondary location. Miller

also discloses that when the bit is not set it the execution address with point to the primary location.

9. Regarding claim 19, Miller taught the method according to claim 17 as described above. Miller further taught confirming that the copying of the boot block is complete prior to pointing the execution address to the primary location (col. 6 line 33 through col. 7 line 7). Specifically, Miller discloses that the copying of boot block is complete when a comparison between the primary location (first region) and the secondary location (second region) produces a match.

10. Regarding claim 25, Miller taught the article according to claim 24 as described above. Miller further taught confirming that the copying of the boot block is complete prior to pointing the execution address to the primary location (col. 6 line 33 through col. 7 line 7). Specifically, Miller discloses that the copying of boot block is complete when a comparison between the primary location (first region) and the secondary location (second region) produces a match, which is interpreted to be confirming that copying is complete.

11. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller, U.S. Patent 6,308,265.

12. Regarding claim 22, Miller taught the system according to claim 6 as described above. Miller teaches maintaining the state of an address bit ("sticky bit") following a power cycle (power failure, power up or a reset col. 5 line 65 through col. 6 line 10). Specifically, Miller discloses using a flag that holds the state of an execution address bit. The flag is set in a latch or a flip-flop and is maintained during a power failure, power up or a reset.

Miller does not expressly disclose using a backup battery for maintaining the state of the address bit. Specifically, Miller is silent as to the power source used to maintain the state of the address bit. Miller suggests using a latch or flip-flop. In order for the state of the latches and flip-flops to be maintained power must be supplied to them. Thus, it is necessary in Miller that another power supply must supply power the latch or flip-flop. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a backup battery to supply power to the latch or flip-flop maintaining the state of the address bit. One of ordinary skill in the art would be motivated to use a battery because batteries are small reliable devices and its power is available during even during a power cycle or power failure.

13. Regarding claim 23, Miller taught the system according to claim 22 as described above. Miller further teaches that jumper may be used for adjusting the address bit (col. 7 line 63 through col. 8 line 34). Miller teaches that the jumper may be used if no hardware exists in the PC to physically cause the adjustment of the address bit.

14. Regarding claims 1-16, the amended claims are addressed as necessitated by amendment.

15. Claims 1-8 and 12-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Miller, U.S. Patent 5,960,445.

16. Regarding claim 1, Miller teaches a method comprising:

a. receiving a boot block into a secondary location (col. 5, lines 44-50);

b. modifying an address bit an execution address to point to the secondary location, wherein the execution address is the address from which a processor executes instruction when a system is turned on (flag used to boot from backup boot block, col. 5, line 65

through col. 6, line 9 and the address line A16 will be inverted according to the flag, col. 7, lines 4-42);

c. maintaining the state of the modified address bit of the execution address following a power cycle (if a reset occurs the flag will still be set, col. 6 lines 4-9).

d. copying the boot block from the secondary location to a primary location (when counter reaches a fixed value, col. 6, lines 53-58); and

e. pointing the execution address to the primary location (the address to primary location must be pointed to in order to allow PC to boot, col. 7, lines 4-42);

17. Regarding claim 2, Miller taught the method according to claim 1, as described above. Miller further taught modifying an address bit of an execution address to point to the secondary location the secondary location further comprising inverting an address bit of the execution address (col. 6 lines 2-10, col. 7 lines 4-42 and col. 8 lines 20-26). Specifically, Miller discloses using a bit to determine where the execution address is pointed. If the bit is set (a "1") the execution address will point to the secondary location. Miller also discloses that when the bit is not set it the execution address with point to the primary location. Therefore, the bit in Miller is inverted from a "0" to a "1". Specifically, Miller uses a flag to determine where the address will point, the address location will correspond to the flag (either FFFFE0000 or FFFFF0000, in which case A16 is inverted depending on the flag, col. 7, lines 36-42).

18. Regarding claim 3, Miller taught the method according to claim 2, as described above. Miller further taught inverting an address bit of the execution address further comprising inverting address bit sixteen of the execution address (col. 8 lines 20-34).

19. Regarding claim 4, Miller taught the method according to claim 1, as described above. Miller further taught confirming that the copying of the boot block is complete prior to pointing the execution address to the primary location (col. 6 line 33 through col. 7 line 7). Specifically, Miller discloses that the copying of boot block is complete when a comparison between the primary location (first region) and the secondary location (second region) produces a match, which is interpreted to be confirming that copying is complete.

20. Regarding claim 5, Miller taught the method according to claim 1, as described above. Specifically, Miller discloses using a bit to determine where the execution address is pointed [col. 6 lines 2-10 and col. 7 lines 4-7]. If the bit is set (a "1") the execution address will point to the secondary location. Miller also discloses that when the bit is not set it the execution address with point to the primary location. Therefore, the bit in Miller is inverted from a "0" to a "1" and is de-inverted when the bit changes from a "1" to a "0".

21. Regarding claim 6, Miller teaches a system comprising:

a. a processor (inherent within the PC, col. 4, lines 19-23);

b. a flash memory comprising a primary location and a secondary location (EPROM, col. 4, lines 45-48);

c. a boot block executed from the primary location, wherein the boot block further:

vi. receives a second boot block in the secondary (boot block code is copied from first to second block region, col. 5, lines 44-50);

vii. modifies an address bit (the boot flag is used to invert an address bit as necessary, col. 7, lines 36-42) of an execution address to point to the secondary

location (flag used to boot from backup boot block, col. 5, line 65 through col. 6, line 9 and col. 7, lines 4-42);

viii. maintains the state of the modified address bit of the execution address following a power cycle (if a reset occurs the flag will still be set, col. 6 lines 4-9).

ix. copies the second boot block to the primary location (when counter reaches a fixed value, col. 6, lines 53-58);

x. points the execution address to the primary location (to allow PC to boot, col. 7, lines 4-7).

22. Regarding claim 7, Miller taught the system according to claim 6, as described above. Miller further teaches an address conversion mechanism for moving the execution address (changing the boot-in-progress flag, col. 7 lines 4-42).

23. Regarding claim 8, Miller taught the system according to claim 6, as described above. Miller further taught a non-volatile storage for storing the second boot block (flash memory is non-volatile memory).

24. Regarding claim 12, Miller teaches a method therefore Miller also teaches the article comprising a medium storing instruction for enabling a processor-based system to:

a. receiving a new boot block into a secondary location (col. 5, lines 44-50);

b. modify an address bit (the boot flag is used to invert an address bit as necessary, col. 7, lines 36-42) of an execution address to point to the secondary location, wherein the execution address is the address from which a processor executes instruction when a system is turned on (flag used to boot from backup boot block, col. 5, line 65 through col. 6, line 9 and col. 7, lines 4-42);

c. maintain the state of the modified address bit of the execution address following a power cycle (if a reset occurs the flag will still be set, col. 6 lines 4-9).

d. copying the new boot block from the secondary location to a primary location (when counter reaches a fixed value, col. 6, lines 53-58); and

e. pointing the execution address to the primary location (the address to primary location must be pointed to in order to allow PC to boot, col. 7, lines 4-42);

25. Regarding claim 13, Miller taught the method according to claim 12, as described above. Miller further taught pointing an execution address to the secondary location further comprising inverting an address bit of the execution address (col. 6 lines 2-10, col. 7 lines 4-42 and col. 8 lines 20-26). Specifically, Miller discloses using a bit to determine where the execution address is pointed. If the bit is set (a "1") the execution address will point to the secondary location. Miller also discloses that when the bit is not set it the execution address with point to the primary location. Therefore, the bit in Miller is inverted from a "0" to a "1".

26. Regarding claim 14, Miller taught the method according to claim 13, as described above. Miller further taught inverting an address bit of the execution address further comprising inverting address bit sixteen of the execution address (col. 8 lines 20-34).

27. Regarding claim 15, Miller taught the method according to claim 12, as described above. Miller further taught confirming that the copying of the boot block is complete prior to pointing the execution address to the primary location (col. 6 line 33 through col. 7 line 7). Specifically, Miller discloses that the copying of boot block is complete when a comparison between the primary location (first region) and the secondary location (second region) produces a match, which is interpreted to be confirming that copying is complete.

28. Regarding claim 16, Miller taught the method according to claim 12, as described above. Specifically, Miller discloses using a bit to determine where the execution address is pointed (col. 6 lines 2-10 and col. 7 lines 4-7). If the bit is set (a "1") the execution address will point to the secondary location. Miller also discloses that when the bit is not set it the execution address with point to the primary location. Therefore, the bit in Miller is inverted from a "0" to a "1" and is de-inverted when the bit changes from a "1" to a "0".

29. Claims 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller, U.S. Patent 6,308,265 in view of Tamori et al., U.S. Patent 5,960,445.

30. Regarding claim 9, Miller taught the system according to claim 6 as described above. Miller does not disclose a network interface card for connecting a system to a network and for downloading the second boot block to the system.

Tamori teaches a network interface card for connecting a system to a network and for downloading the second boot block to the system (BIOS code, col. 7, lines 3-7). Tamori suggests to those of ordinary skill in the art that updating the boot block by downloading the boot block over a network would have the advantage of easily having access the latest boot block, which would increase usability, functionality and reliability over other methods of obtaining the boot block.

It would have been obvious to one of ordinary skill in the art, having the teachings of Miller and Tamori before them at the time the invention was made to modify Miller to include the network interface card of Tamori to obtain downloading the boot block over a network.

One of ordinary skill would have been motivated to make this modification in order to achieve the advantage of easily having access to the latest boot block, which would increase usability, functionality and reliability over other methods of obtaining the boot block in view of the teachings of Tamori.

31. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller, U.S. Patent 6,308,265.

32. Regarding claim 10, Miller taught the system according to claim 6 as described above. Miller teaches maintaining the state of an address bit ("sticky bit") following a power cycle (power failure, power up or a reset col. 5 line 65 through col. 6 line 10). Specifically, Miller discloses using a flag that holds the state of an execution address bit. The flag is set in a latch or a flip-flop and is maintained during a power failure, power up or a reset.

Miller does not expressly disclose using a backup battery for maintaining the state of the address bit. Specifically, Miller is silent as to the power source used to maintain the state of the address bit. Miller suggests using a latch or flip-flop. In order for the state of the latches and flip-flops to be maintained power must be supplied to them. Thus, it is necessary in Miller that another power supply must supply power the latch or flip-flop. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a backup battery to supply power to the latch or flip-flop maintaining the state of the address bit. One of ordinary skill in the art would be motivated to use a battery because batteries are small reliable devices and its power is available during even during a power cycle or power failure.

33. Regarding claim 11, Miller taught the system according to claim 6 as described above. Miller further teaches that jumper may be used for adjusting the address bit (col. 7 line 63 through col. 8 line 34). Miller teaches that the jumper may be used if no hardware exists in the PC to physically cause the adjustment of the address bit.

Response to Arguments

34. All rejections of claim limitations as filed prior to Amendment dated 4/11/05 not argued in their entirety or substantively in the response to the prior Office action have been conceded by Applicant and the rejections are maintained from henceforth.

35. Applicant's arguments filed 4/11/05 have been fully considered but they are not persuasive.

36. Applicants argue in substance that the grounds of rejections for claims 17-21 and 24-25 have not changed and request a new non-final action so that applicants have a fair opportunity to reply. However, claims 17-21 and 24-25 were amended to include new limitations. The last rejection was necessitated by amendment and it is believed that the new limitations were addressed in the rejection. Therefore and new non-final action is not believed necessary as the amended claims have been given a fair opportunity for reply.

37. The examiner appreciates the notice of an editorial error in the §102 rejection wherein the Patent Number should have been 6,308,265 rather than 5,960,445.

38. Applicants argue in substance that Miller does not teach or suggest modifying an address bit of the execution address. The examiner disagrees. Applicants are directed to col. 7, lines 36-42. Miller discloses that an address bit is inverted to point to either the first or second address

according to a whether a flag is set or not set. Therefore, Miller does disclose modifying an address bit of the execution address. Because the flag is maintained during a power cycle the address bit is also maintained during a power cycle.

39. Applicants also argue in substance that motivation for the rejection of claims 10 and 11 come impermissibly from the teachings of the present specification and is thus improper hindsight reasoning. As addressed in the last rejection, Miller uses a flag, or sticky bit to cause an address bit to be maintained following a power cycle. Miller suggests using a latch or flip-flop. In order for the state of a latch or flip-flop to be maintained it is inherent that power must be supplied to them. The power supply would have to independent from the main power supply because the main power supply is cycled to an off state as suggested by Miller. Miller does not explicitly disclose the type of power supply used to supply power to the latch or flip-flop. However, batteries are known those of ordinary skill in the art. Batteries have often been used as back up power supplies. Batteries are small and reliable. It would have been obvious to one ordinary skill in the art, having the teachings of Miller and the well known knowledge of using batteries as a backup power supply to maintain the state of latch or flip-flop. One of ordinary skill in the art would have been motivated to make use of a battery because batteries are small reliable devices and its power is available during even during a power cycle or power failure.

Also, regarding claim 11, applicants argue in substance that the rejection appears to come impermissibly from the teachings of the present application is thus also improper hindsight reasoning. The applicants are directed to col. 7, line 63 through col. 8, line 34, where Miller teaches that the jumper may be used if no hardware exists in the PC to physically cause the adjustment of the address bit.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Conclusion

40. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (571) 272-3677. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Trujillo
June 28, 2005

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